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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/888,271	Applicant(s) GREENBERG, ROBERT Y.	
	Examiner Trang U. Tran	Art Unit 2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-42 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-42 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-4, 6, 11, 13-22, 25-26, 28-32, 34-38 and 40-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Cappels, Sr. (US Patent No. 5,731,843).

In considering claim 1, Cappels, Sr. discloses all the claimed subject matter, note 1) the claimed a phase locked loop circuit adapted to generate a phase locked loop clock responsive to a reference signal is met by the pixel sampling clock 55 which is a conventional phase-locked loop using a programmable divider and coupled to the horizontal sync pulse (Fig. 3, col. 4, lines 35-42), 2) the claimed an edge detector circuit adapted to generate an edge pulse signal corresponding to a transition of an analog data signal is met by the differentiator 52 and the threshold detector 44 which is function together to detect voltage transitions between pixel instructions, also called pixels edges (Fig. 3, col. 4, lines 42-59), 3) the claimed a phase detector circuit adapted to identify a phase of the phase locked loop clock associated to the transition of the analog data and thereby generate a phase adjust signal is met by the phase comparator 46 and the microprocessor 48 (Fig. 3, col. 4, line 60 to col. 5, line 27), and 4) the claimed a phase adjust circuit adapted to generate a pixel clock by adjusting the phase of the phase locked loop clock responsive to the phase adjust signal is met by the phase adjuster 50

which produces an adjusted pixel sampling clock 64 that matches the phase of the video signal 52 (Figs. 3 and 4, col. 5, line 15 to col. 6, line 31).

In considering claim 3, the claimed wherein the reference signal is a horizontal synchronization signal is met by the pixel sampling clock 55 which is a conventional phase-locked loop using a programmable divider and coupled to the horizontal sync pulse (Fig. 3, col. 4, lines 35-42).

In considering claim 4, the claimed wherein the edge detector is adapted to generate an edge pulse corresponding to the transition of the analog data signal above a predetermined threshold is met by the differentiator 95 and the threshold detector 100 which is function together to produce the pulse signal if the applied voltage pulse exceeding a predetermined threshold voltage (Figs. 3 and 5, col. 2, lines 5-28 and col. 6, lines 32-57).

In considering claim 6, the claimed wherein the edge detector is adapted to generate an edge pulse corresponding to a rising, falling, or both rising and falling edges of the analog data signal is met by the voltage transition location 20 which occurs between a change in voltage levels and between discrete pixel intensities 19 on video signal 12 (Fig. 1, col. 3, lines 6-43).

In considering claim 11, Cappels, Sr. discloses all the claimed subject matter, note 1) the claimed wherein the phase adjust circuit generates a plurality of delayed clock signals by delaying the phase locked loop clock is met by is met by the phase adjuster (phase shift of Fig. 4) 50 which produces an adjusted pixel sampling clock 64 that matches the phase of the video signal 52 (Figs. 3 and 4, col. 5, line 15 to col. 6, line

31), 2) the claimed wherein the phase detector comprises: a phase hit detector adapted to generate a plurality of phase hit enable signals corresponding to the plurality of delayed clock signals and assert one of the phase hit enable signals responsive to the edge pulse signal is met by the hit detection process (Fig. 5, col. 4, line 60 to col. 5, line 27 and col. 6, line 58 to col. 7, line 37), and 3) the claimed a phase hit counter adapted to count asserted phase hit enable signals for each of the delayed clock signals over a predetermined time is met the microprocessor 48 stores in memory 49 a number representing the total hits for that specific phase (col. 5, lines 3-27).

In considering claim 13, the claimed wherein the phase hit detector comprises: a plurality of flip-flop circuits corresponding to the plurality of delayed clock signals adapted to generate a corresponding plurality of phase out signals, and a comparison circuit adapted to comparing the plurality of phase out signals is met by the comparator 99 which includes a one-shot pulse generator 81 and latches (flip-flops) 82 and 84 (Fig. 5, col. 6, line 58 to col. 7, line 37).

In considering claim 14, the claimed wherein the comparison circuit is adapted to compare adjacent phase out signals is met by the comparator 99 which includes a one-shot pulse generator 81 and latches (flip-flops) 82 and 84 (Fig. 5, col. 6, line 58 to col. 7, line 37).

In considering claim 15, the claimed wherein the phase hit counter comprises: an enable signal adapted to enable counting of asserted phase hit enable signals is met by the Q-output pulse 108 from the one-shot pulse generator 81 is true, data line 112 is set high, indicating that a "hit", a sampling edge in close temporal proximity to a video

transition, has taken place (Fig. 5, col. 6, line 58 to col. 7, line 37), and a clear signal adapted to clear the phase hit counter is met by the NOT-Q output 118 of one-shot pulse generator 81, the latch 82 is reset to await for the next edge detection (Fig. 5, col. 6, line 58 to col. 7, line 37) .

In considering claim 16, the claimed comprising: a phase count analysis circuit adapted to generate phase and frequency adjust signals by analyzing the count of asserted phase hit enable signals is met by the microprocessor 48 which calculates a hit percentage for each varies phase and the hit percentage is the number of hits for a given number of video edges at a given phase to obtain which phase is the maximum number of hits, then the microprocessor 48 can determine the phase of the sampling clock with respect to the horizontal synchronization pulse that will provide the optimum sampling of the incoming video signal 52 (Fig. 4, col. 5, line 15 to col. 6, line 31).

In considering claim 17, the claimed comprising an auto calibration circuit adapted to align the analog data signal with the pixel clock is met by the automatically adjusting the pixel sampling clock frequency and phase to match the frequency and phase of the pixel clock used to generate an incoming video signal (col. 1, lines 60-64).

Claim 18 is rejected for the same reason as discussed in claim 1.

Claim 19 is rejected for the same reason as discussed in claim 4.

Claim 20 is rejected for the same reason as discussed in claim 6.

Claim 21 is rejected for the same reason as discussed in claim 17.

Claim 22 is rejected for the same reason as discussed in claim 7.

Claim 25 is rejected for the same reason as discussed in claim 11.

Claim 26 is rejected for the same reason as discussed in claim 15.

Claim 28 is rejected for the same reason as discussed in claim 16.

In considering claim 29, the claimed comprising a phase locked loop circuit adapted to derive the clock signal from the reference signal responsive to a frequency adjust signal is met by the pixel sampling clock 55 which is a conventional phase-locked loop using a programmable divider and coupled to the horizontal sync pulse (Fig. 3, col. 4, lines 35-42).

Claim 30 is rejected for the same reason as discussed in claim 16.

The method claim 31 is rejected for the same reason as discussed in the apparatus claim 1.

Claim 32 is rejected for the same reason as discussed in claim 29.

Claim 34 is rejected for the same reason as discussed in claim 4.

Claim 35 is rejected for the same reason as discussed in claim 6.

In considering claim 36, the claimed wherein detecting a transition includes generating an edge pulse responsive to the transition and wherein asserting a clock phase hit includes comparing the edge pulse with each of the clock phase is met by the hit detection process (Fig. 5, col. 4, line 60 to col. 5, line 27 and col. 6, line 58 to col. 7, line 37).

In considering claim 37, the claimed wherein asserting the clock phase hit includes generating a plurality of clock phase hit signals corresponding to the plurality of clock phases and asserting only the clock phase hit signal closest to the transition is

met by the hit detection process (Fig. 5, col. 4, line 60 to col. 5, line 27 and col. 6, line 58 to col. 7, line 37).

Claim 38 is rejected for the same reason as discussed in claim 11.

Claim 40 is rejected for the same reason as discussed in claim 15.

In considering claim 41, the claimed wherein counting includes generating a count for each of the clock phases and wherein counting comprises: examining the count; and adjusting the frequency of the pixel clock if the count exceeds a predetermined number is met by is met by the microprocessor 48 can determine the phase of the sampling clock with respect to the horizontal synchronization pulse that will provide the optimum sampling of the incoming video signal 52 by determining which phase obtains a maximum number of hits and the microprocessor 48 using line 67 to vary the pixel clock frequencies via the pixel clock 55 until a single, distinct, optimum setting is obtained (Fig. 4, col. 5, line 15 to col. 6, line 31).

In considering claim 42, the claimed wherein adjusting the frequency of the pixel clock comprises: changing the frequency of the clock signal; clearing the count; enabling the count; repeating the counting, examining, and adjusting if the count exceeds a predetermined number is met by is met by the microprocessor 48 can determine the phase of the sampling clock with respect to the horizontal synchronization pulse that will provide the optimum sampling of the incoming video signal 52 by determining which phase obtains a maximum number of hits and the microprocessor 48 using line 67 to vary the pixel clock frequencies via the pixel clock 55 until a single, distinct, optimum setting is obtained (Fig. 4, col. 5, line 15 to col. 6, line 31).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 12, 27 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cappels, Sr. (US Patent No. 5,731,843)

In considering claim 5, Cappels, Sr. discloses all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the threshold is programmable. The capability of using the threshold is programmable is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the old and well known of using the threshold is programmable into Cappels, Sr.'s system in order to accurately detect the edge pulse signal because programmable device can easily adjust the threshold level to appropriate level.

In considering claim 12, Cappels, Sr. discloses all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the predetermined time is a number of image scan lines. The capability of using the predetermined time is a number of image scan lines is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the old and well known of using

the predetermined time is a number of image scan lines into Cappels, Sr.'s system since it merely amounts to selecting an alternative equivalent edge detector.

Claim 27 is rejected for the same reason as discussed in claim 12.

Claim 39 is rejected for the same reason as discussed in claim 12.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cappels, Sr. (US Patent No. 5,731,843) in view of Koike et al (US Patent No. 6,538,648 B1).

In considering claim 2, Cappels, Sr. discloses all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the phase locked loop circuit comprises: a phase detector adapted to receive the reference signal; a loop filter coupled to the phase detector; a voltage controlled oscillator coupled to the loop filter; a feedback loop adapted to receive the phase locked loop clock and provide a feedback signal responsive to a frequency adjust signal. Koike et al teach that the PLL circuit 40 comprises a phase detection unit 41, an LPF (Low pass Filter) 42, a VCO (Voltage Control Oscillator) 43, and a frequency divider 44, as is well known (Fig. 2, col. 6, lines 46-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the old and well known PLL as taught by Koike et al into Cappels, Sr.'s system in order to generate the clock signal that is synchronized with the local frequency oscillator.

6. Claims 7-10, 23-24 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cappels, Sr. (US Patent No. 5,731,843) in view of Ichiraku (US Patent No. 6,097,379).

In considering claim 7, Cappels, Sr. discloses all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the phase adjust circuit is adapted to adjust the phase of the pixel clock by delaying the reference signal. Ichiraku teaches that as is shown in Fig. 3, the phase adjusting circuit 2 of the present invention is provided with: a sampling clock generating circuit for detection 21, into which a standard clock (PCLK) which is synchronized with a horizontal synchronizing signal is inputted, and which divides this standard clock (PCLK) into a number m (a positive integer) of standard clocks, and which applies, with respect to these standard clocks, a delay amount proportional to the amount of the cycle thereof divided by m, and which generates and outputs, in stages, a number m of sampling clocks for detection (DPCLK [0,1,2,...,m]) having different phases (Fig. 3, col. 8, line 43 to col. 9, line 40). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the delay clocks (DPCLK [0,1,2,...,m]) having different phases as taught by Ichiraku into Cappels, Sr.'s system in order to accurately produce the sampling clock signal having an appropriate phase for sampling pixel data of the video signal.

In considering claim 8, Cappels, Sr. discloses all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the phase adjust circuit is adapted to adjust the phase of the pixel clock by delaying the phase locked loop clock. Ichiraku teaches that as is shown in Fig. 3, the phase adjusting circuit 2 of the present invention is provided with: a sampling clock generating circuit for detection 21, into which a standard clock (PCLK) which is synchronized with a

horizontal synchronizing signal is inputted, and which divides this standard clock (PCLK) into a number m (a positive integer) of standard clocks, and which applies, with respect to these standard clocks, a delay amount proportional to the amount of the cycle thereof divided by m, and which generates and outputs, in stages, a number m of sampling clocks for detection (DPCLK [0,1,2,...,m]) having different phases (Fig. 3, col. 8, line 43 to col. 9, line 40). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the delay clocks (DPCLK[0,1,2,...,m]) having different phases as taught by Ichiraku into Cappels, Sr.'s system in order to accurately produce the sampling clock signal having an appropriate phase for sampling pixel data of the video signal.

In considering claim 9, Ichiraku discloses the claimed wherein the phase adjust circuit comprises: a clock delay circuit adapted to generate a plurality of delayed clock signals by delaying the phase locked loop clock is met by the delay clocks (DPCLK [0,1,2,...,m]) having different phases (Fig. 3, col. 8, line 43 to col. 9, line 40), and the claimed a multiplexer adapted to select one of the plurality of delayed clock signals as the pixel clock responsive to a phase adjust signal is met by the selecting circuit 22 which selects the appropriate sampling clock for detection and outputs this as the sampling clock (SCLK) to the pixel data sampling circuit (Fig. 3, col. 8, line 43 to col. 9, line 40).

In considering claim 10, the claimed wherein the clock delay circuit comprises an n-stage delay locked loop, each stage generating a corresponding delayed clock phase, each delayed clock phase being 360/n degrees out of phase is met by the delay clocks

(DPCLK [0,1,2,...,m]) having different phases (Fig. 3, col. 8, line 43 to col. 9, line 40) of Ichiraku.

Claim 23 is rejected for the same reason as discussed in claim 9.

Claim 24 is rejected for the same reason as discussed in claim 10.

Claim 33 is rejected for the same reason as discussed in claim 9.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Abe et al. (US Patent No. 5,940,136) disclose dot clock reproducing method and dot clock reproducing apparatus using the same.

Levantovsky et al. (US Patent No. 6,522,365 B1) disclose method and system for pixel clock recovery.

Morita (US Patent No. 6,621,480 B1) discloses phase adjuster, phase adjusting method and display device.

Yoneno (US Patent No. 6,304,296 B1) discloses method and apparatus for adjusting dot clock signal.

Vidovich (US Patent No. 6,226,045 B1) discloses dot clock recovery method and apparatus.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Trang U. Tran** whose telephone number is **(703) 305-0090.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **John W. Miller,** can be reached at **(703) 305-4795.**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 308-HELP.

MICHAEL H. LEE
PRIMARY EXAMINER

TT TT
November 11, 2003